

CLAIMS

What is claimed is:

1. A system comprising:
a trigger-matching logic to capture an incoming cycle and determine if the captured incoming cycle matches one or more of trigger conditions; and
a control logic coupled to the trigger-matching logic to select a set of instructions upon detection of at least one matched trigger condition and to execute operations as specified by the selected set of instructions, wherein the set of instructions is selected based on the at least one matched trigger condition.
2. The system of claim 1, wherein the trigger-matching logic and the control logic are incorporated within an Input/Output (I/O) chip.
3. The system of claim 1, wherein the control logic can execute an operation which involves logically combining a selected operand entry with a selected register containing information from the captured cycle.
4. The system of claim 2, wherein the control logic can execute an operation which causes a new cycle to be created and forwarded to a downstream bus of the I/O controller.
5. The system of claim 1, wherein the control logic can execute an operation which involves modifying the captured incoming cycle.
6. The system of claim 1, wherein the control logic can execute an operation which causes a timed delay or a conditional delay to be inserted.
7. A method comprising:
receiving an incoming cycle;
loading information from the received cycle into a first register;
comparing the information stored in the first register with trigger conditions;
selecting a sequence of instructions based on a matched trigger condition; and
executing the selected instructions sequentially.

8. The method of claim 7, wherein the incoming cycle is received within an I/O controller chip.

9. The method of claim 7, wherein executing of the instructions comprises:

logically combining a selected operand entry with a selected register containing information captured from the received cycle.

10. The method of claim 8, wherein executing the instructions comprises: generating a new cycle and forwarding the new cycle to a downstream bus of the I/O controller chip.

11. The method of claim 7, wherein executing the instructions comprises: modifying a cycle type section of the incoming cycle.

12. The method of claim 7, wherein executing the instructions comprises: modifying an address section of the incoming cycle.

13. The method of claim 7, wherein executing the instructions comprises: modifying a data section of the incoming cycle.

14. The method of claim 7, wherein executing the instructions comprises: inserting a timed delay or a conditional delay.

15. A patch module comprising:
a cycle capture unit to capture request cycles forwarded by a processor;
a plurality of trigger registers to store trigger conditions;
a trigger comparator coupled between the cycle capture unit and the trigger registers to determine if information associated with the captured request cycle matches trigger conditions stored in the trigger registers;
an instruction storage to store instructions;

an instruction select unit to select a set of instructions from the instruction storage based on one or more of matched trigger conditions;

an instruction execution unit to execute the set of instructions selected by the instruction select unit.

16. The patch module of claim 15, wherein the patch module is embedded within an I/O controller chip and can be programmed by a user to workaround conditions and defects existing in the I/O controller chip.

17. The patch module of claim 15, wherein the instruction execution unit can execute an instruction that comprises:

a first field to specify a type of operation to be performed, wherein the type of operations identified by the first field includes (1) timed delay operation, (2) conditional delay operation, (3) generating new cycle operation, and (4) modifying the capture request cycle operation; and

a second field to specify whether or not a cycle generated by the instruction is to be forwarded to downstream bus.

18. The patch module of claim 15, wherein the instruction execution unit can execute an instruction that comprises:

a third field to select a register to modify;

a fourth field to select an operand entry from an operand array; and

a fifth field to select a logic gate for combining the selected register with the selected operand entry.

19. The patch module of claim 17, wherein the captured incoming cycle is a non-posted cycle.

20. The patch module of claim 19, wherein the instruction execution unit can execute an instruction that comprises:

a fifth field to specify whether a completion queue is to be loaded with unmodified header information from the captured non-posted cycle or loaded with

modified header information associated with modified request cycle that is generated by the control logic; and

a sixth field to specify whether or not a completion associated with the capture request cycle is to be discarded.

21. A machine-readable medium that provides instructions, which when executed by a processor cause the processor the perform operations comprising:
receiving an incoming cycle;
comparing information obtained from the incoming cycle to trigger conditions;
generating a sequence of instructions to be executed in response to a matched trigger condition; and
executing the generated instructions sequentially.

22. The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:
generating a new cycle and forwarding the new cycle to a downstream bus of an I/O controller chip.

23. The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:
modifying a cycle type section of the incoming cycle.

24. The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:
modifying an address section of the incoming cycle.

25. The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:
modifying a data section of the incoming cycle.

26. The machine-readable medium of claim 21, wherein the operations performed by the processor further comprise:
inserting a timed delay or a conditional delay.